CLAIMS

1. A liquid crystal driving circuit in which a plurality of source driver circuit devices for driving a liquid crystal element are arranged on a liquid crystal panel, the liquid crystal driving circuit comprising:

a reference voltage production circuit for producing a plurality of reference voltages for driving the liquid crystal element; and

a plurality of reference voltage wires for supplying the plurality of reference voltages, produced by the reference voltage production circuit, to the source driver circuit devices, respectively, the reference voltage wires extending through an area on the liquid crystal panel and an area on each of the source driver circuit devices.

2. The liquid crystal driving circuit of claim 1, each of the source driver circuit devices including:

a plurality of in-chip reference voltage wires extending from one end to the other end of the source driver circuit device for supplying a plurality of reference voltages different from one another;

the same number of branch reference voltage wires branching off from the plurality of in-chip reference voltage wires, respectively;

the same number of buffers for receiving and then outputting reference voltages supplied from the plurality of branch reference voltage wires, respectively; and

a selection circuit for selecting, as a voltage for driving the liquid crystal element, one of the reference voltages supplied from the plurality of buffers.

3. A semiconductor integrated circuit device provided in a liquid crystal module and carrying thereon a source driver circuit for driving a liquid crystal element, wherein the source driver circuit includes:

a plurality of in-chip reference voltage wires extending from one end to the other end of the semiconductor integrated circuit device for supplying a plurality of reference voltages different from one another;

the same number of branch reference voltage wires branching off from the plurality of in-chip reference voltage wires, respectively;

the same number of buffers for receiving and then outputting reference voltages supplied from the plurality of branch reference voltage wires, respectively; and

a selection circuit for selecting, as a voltage for driving the liquid crystal element, one of the reference voltages supplied from the plurality of buffers.

4. The semiconductor integrated circuit device of claim 3, further including a subdivided voltage production circuit for receiving an output voltage from each of the buffers so as to produce subdivided voltages obtained by subdividing the plurality of reference voltages, and then outputting the subdivided voltages to the selection circuit,

wherein the selection circuit selects one of the subdivided voltages. (p. 5-6)

5. The semiconductor integrated circuit device of claim 3 or 4,

wherein the buffer has an offset canceling function for reducing a potential difference between an input voltage and an output voltage. (prior Art IDS)

6. The semiconductor integrated circuit device of claim 5, wherein the buffer includes:

an operator for receiving an input voltage to the buffer at one terminal and an output voltage of the operator itself at ~~the other terminal~~ 112, and operating so that the output voltage is equal to the input voltage;

a capacitor including a first electrode and a second electrode for storing a charge corresponding to a voltage difference between the input voltage and the output voltage;

an input-side node for introducing the input voltage to the operator;

a first node connected to the first electrode of the capacitor;

a second node connected to the second electrode of the capacitor;

a third node for receiving the output voltage from the operator;

a first switching element provided between the second node and the third node;

a second switching element provided between the first node and a node on an input side of the operator; and

a third switching element provided between the first node and the third node.

7. The semiconductor integrated circuit device of claim 6, further including a closed circuit added to the second node, the closed circuit including therein a fifth switching element for compensating for an electric change in the second node due to switching of the first switching element.

8. The semiconductor integrated circuit device of claim 5, wherein:

the buffer includes two buffering circuits arranged in parallel to each other between an input-side node for receiving an externally produced reference voltage as the input voltage and an output-side node for sending out the output voltage; and

each of the buffering circuits includes:

an operator for receiving the input voltage at one terminal and an output voltage of the operator itself at the other terminal, and operating so that the output voltage is equal to the input voltage;

a capacitor including a first electrode and a second electrode for storing a charge corresponding to a voltage difference between the input voltage and the output voltage;

a first node connected to the first electrode of the

capacitor;

a second node connected to the second electrode of the capacitor;

a third node for receiving an output signal from the operator;

a first switching element provided between the second node and the third node;

a second switching element provided between the first node and the input-side node;

a third switching element provided between the first node and the output-side node; and

a fourth switching element provided between the third node and the output-side node.

9. A reference voltage buffering circuit provided in a source driver circuit for driving a liquid crystal element of a liquid crystal module, wherein:

the reference voltage buffering circuit comprises two buffering circuits arranged in parallel to each other between an input-side node for receiving an externally produced reference voltage as an input voltage and an output-side node for sending out an output voltage; and

each of the buffering circuits includes:

an operator for receiving the input voltage at one terminal and an output voltage of the operator itself at the other terminal, and operating so that the output voltage is equal to the input voltage;

a capacitor including a first electrode and a second electrode for storing a charge corresponding to a voltage difference between the input voltage and the output voltage;

a first node connected to the first electrode of the capacitor;

a second node connected to the second electrode of the capacitor;

a third node for receiving an output signal from the operator;

a first switching element provided between the second node and the third node;

a second switching element provided between the first node and the input side of the operator;

a third switching element provided between the first node and the output-side node; and

a fourth switching element provided between the third node and the output-side node.

10. The reference voltage buffering circuit of claim 9, further comprising a closed circuit added to the second node, the closed circuit including therein a fifth switching element for compensating for an electric change in the second node due to switching of the first switching element.

11. A method for controlling a reference voltage buffering circuit, including two buffering circuits arranged in parallel to each other, each of the buffering circuits including: an operator provided between an input-side node

and an output-side node for operating so that an output voltage is equal to an input voltage; a capacitor including a first electrode and a second electrode; a first node connected to the first electrode of the capacitor; a second node connected to the second electrode of the capacitor; a third node for receiving an output signal from the operator; a first switching element provided between the second node and the third node; a second switching element provided between the first node and the input side of the operator; a third switching element provided between the first node and the output-side node; and a fourth switching element provided between the third node and the output-side node, wherein:

in each of the buffering circuits, in an output mode in which a reference voltage is output from the buffering circuit, the third and fourth switching elements are placed in a conductive state while the first and second switching elements are placed in a non-conductive state; and

in a charge storing mode in which the capacitor of the buffering circuit stores a charge, the third and fourth switching elements are placed in a non-conductive state while the first and second switching elements are placed in a conductive state.

12. The method for controlling a reference voltage buffering circuit of claim 11, wherein:

the reference voltage buffering circuit further includes a closed circuit added to the second node, the

closed circuit including therein a fifth switching element for canceling out an electric change in the second node due to switching of the first switching element; and

when the first switching element is switched between a conductive state and a non-conductive state from one to another, the fifth switching element is switched reversely in an interlocking manner.

13. The method for controlling a reference voltage buffering circuit of claim 11 or 12, wherein:

when switching from a state where one of the two buffering circuits is in the output mode while the other buffering circuit is in the charge storing mode to another state where the one buffering circuit is in the charge storing mode while the other buffering circuit is in the output mode,

the third and fourth switching elements of the other buffering circuit are switched to a conductive state after the third and fourth switching elements of the one buffering circuit are switched to a non-conductive state.

14. The method for controlling a reference voltage buffering circuit of claim 13, wherein:

when the third and fourth switching elements of the one buffering circuit are switched to a non-conductive state, the third switching element is switched to a non-conductive state after the fourth switching element is switched to a non-conductive state; and

when the third and fourth switching elements of the other buffering circuit are switched to a conductive state, the fourth switching element is switched to a conductive state after the third switching element is switched to a conductive state.